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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/645,922 | 08/20/2003 | Jung-Hwan Choi | 9898-296 | 9301 |

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| EXAMINER | |
|---|---|
| TRAN, ANH Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/645,922 | CHOI, JUNG-HWAN | |
| | Examiner | Art Unit | |
| | Anh Q. Tran | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,11-20 and 22-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-14,17-23,28,29 and 34-37* is/are rejected.

7)☒ Claim(s) *15,16,24-27 and 30-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Zerbe (6,396,329).

Zerbe shows:

1. A semiconductor device (Fig. 30, 40, 41, & 52B, comprising:

a transmitter (Fig. 30) capable of encoding first (LSB Odd data and Even data) and second input signals (MSB Odd and Even data) as a plural-bit symbol signal responsive to first (CLK) and second clocks (CLB), respectively, the first clock being out of phase from the second clock (col. 36, lines 36-38); and

a receiver (Fig. 40) capable of generating first (MSB even and odd) and second output signals (LSB even and odd) by decoding the symbol signal responsive to third (Precharge_even and fourth (Precharge_odd) clocks, respectively, and capable of generating first and second even and odd data.

2. The semiconductor device of claim 1 where the plural-bit symbol signal is at least two bit data (It is four bit data).

3-6. The semiconductor device of claim 2 where the at least two bit data is a three level data (col. 48, lines 6-12).

8. The semiconductor device of claim 1 where the fourth clock is 90 degrees out of phase from the third clock (Figure 24 shows each receiver 780-1 to 780-4 as comprising even and odd data, furthermore the clock phase is 90 degrees out of phase relatively to one another, col. 31, lines 12-15 and lines 58-64).

7 & 19. the limitations of the claims rejected as above claim 8, because 8 PAM or 16 PAM drivers can be expanded (col. 36, lines 11-13) which required parallel drivers connected as Fig. 24 for transmitting signal and the 90 degrees out of phase relatively to one another in each driver.

9. The semiconductor device of claim 1 where the symbol signal comprises a plurality of symbols.

11. The semiconductor device of claim 1 where the transmitter comprises:

a first transmitting (958, Fig. 30) circuit capable of generating a first transmitting signal by manipulating the first input signal responsive to the first clock (CLK);

a second transmitting circuit (954) capable of generating a second transmitting signal by manipulating the second input signal responsive to the second clock (CLKB); and a superposition node (956) capable of generating the symbol signal by super-positioning the first and second transmitting signals.

12-13. The semiconductor device of claim 1 where the receiver comprises:

a first receiving circuit (333-EVEN, Fig. 7) capable of generating the first output signal by manipulating the symbol responsive to the third (Precharge_even, Fig. 50) and

a fifth clocks (Precharge_even_b, Fig. 50), the fifth clock being out of phase from the third clock (180 degree); and

a second receiving circuit (333-ODD) capable of generating the second output signal by manipulating the symbol signal responsive to the fourth (Precharge_odd, Fig. 50) and a sixth clocks (Precharge_odd_b, Fig. 50), the sixth clock being out of phase from the fourth clock (180 degree).

14. The semiconductor device of claim 12 where the first receiving circuit (1112 A, Fig. 41) is capable of generating the first even (MSBeven) and odd (MSBodd) data responsive to the third (Precharge_even, Fig. 50) and fifth clocks (Precharge_odd, Fig. 50), respectively; and

where the second receiving circuit (1114A, Fig. 41) is capable of generating the second even (LSBeven) and odd (LSBodd) data responsive to the fourth (Precharge_even_b, Fig. 50) and sixth clocks (Precharge_odd_b, Fig. 50), respectively.

15. The semiconductor device of claim 14 where the first receiving circuit comprises:

a first detector capable of generating the first even and odd data according lo a medium reference voltage;

17-18, 20, 22-23, 28. The limitations are rejected as above claims.

29. The receiver of claim 28 where the first receiver (1112A, Fig. 41) is capable of receiving the second even (any one of signals A-Deven) and odd (any one of signals A-Dodd) data; and

where the second receiver (1114A) is capable of receiving the first even (any one of signals A-Deven) and odd data (any one of signals A-Dodd).

34. A transmitter, comprising:

a first driver (780-1, Fig. 24) capable of generating first transmit data responsive to a first transmitting clock (Φ1);

a second driver (780-2) capable of generating second transmit data responsive to a second transmitting clock, the first transmitting clock being out of phase relative to the second transmitting clock (col. 31, lines 12-15); and

a superposition node (VOUT, VOUTB) adapted to superposition the first and second transmit data to generate multi-bit symbol data.

35. The transmitter of claim 34 where the symbol data represents at least two bit data.

36. The transmitter of claim 34 where the second transmitting clock is 90 degree out of phase of the first transmitting clock (col. 31, lines 12-15).

37. The transmitter of claim 34 where the second transmitting clock is half bit time (90 degree out of phase) out of phase of the first transmitting clock.

***Allowable Subject Matter***

3. Claims 15-16, 24-27, 30-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**ANH Q. TRAN**
**PRIMARY EXAMINER**

6/30/05